62. A data processor performing data processing based on an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of a plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein the plurality of registers includes at least one register storing an address exceeding 16 bits.

63. A data processor performing data processing based on an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of a plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein at least one instruction is further followed by a numeric code of more than 16 bits.

64. A data processor performing data processing based on an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of a plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein a first register and a second register are included in the plurality of regsiters, and

a judgement of which one of sign-extending and zero-extending is to be performed on operand data is made depending on which of the first register and the second register is designated as the destination operand in the instruction.

65. A data processor performing data processing based on an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of a plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein an address register and a data register are included in the plurality of registers, and

an address stored in the address register is longer than data stored in the data register.

Add A2

Add D1